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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/691,004	10/18/2000	Leonard Forbes	303.324US4	4509

7590 05/20/2002

Schwegman, Lundberg, Woessner & Kluth, P.A.
P.O.Box 2938
Minneapolis, MN 55402

EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 05/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/691,004	FORBES ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 29 April 2002.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 36-45,56-85 and 98-100 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 36-45, 56-85, and 98-100 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 36-45, 56-85, and 98-100 in Paper No. 5 is acknowledged. In the same Paper No. 5 claims 46-55 and 86-97 were canceled.

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statement of Paper No. 2, the Supplemental Information Disclosure Statement of Paper No. 6. The Information Disclosure Statement of October 18, 2000 has been considered to the extent the literature cited therein was available, i.e., the patent literature, both domestic and foreign.

Applicant is requested to send the non-patent literature items so as to enable the examiner to fully consider said non-patent literature items.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. ***Claim 40*** is rejected under 35 U.S.C. 102(e) as being anticipated by Forbes et al (5,989,958). Forbes et al teach a transistor comprising: a source region 102, drain region 104, and channel region 108, and a floating gate 110 formed of silicon carbide (cf. abstract, second sentence and title) separated from a control gate 114 by an insulating layer 112 (see Derwent summary, for instance, or column 2, line 64 – column 3, line 10). The floating gate has a reduced electron affinity to allow for data erase operations with lower voltages (cf. abstract, final sentence), and hence the stoichiometric parameter x in $Si_{1-x}C_x$ has the value x=0.5 evidently because this value corresponds to a better value for the barrier energy, than the value x=0 would (pure silicon). In conclusion, Forbes et al anticipate claim 40.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. ***Claim 40*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara (5,798,548) in view of Weitzel et al (5,661,312) and Hamakawa et al (JP357126175A). Fujiwara teaches a transistor (cf. front figure) comprising a source region 2, a drain region 2, a channel region 3 between source and drain regions, and an electrically

floating gate 5 separated from the channel region by an insulator 4 (cf. column 3, lines 60-67 and column 4, lines 1-5), the floating gate formed of polysilicon (cf. column 4, lines 4-5); and a control gate 7 (cf. column 4, lines 7-10), separated from the floating gate by an intergate dielectric 6 (cf. column 4, line 6). Fujiwara does not necessarily teach the floating gate to be formed of silicon carbide compound $Si_{1-x}C_x$ with x between 0 and 1. However, silicon carbide has long been used in the art of MOSFET devices to achieve better breakdown performance, as witnessed by Weitzel et al (cf. abstract and claim 10), while in the related art of photoelectric conversion it has long been known that $Si_{1-x}C_x$ can be selected as an excellent material for obtaining high electronic conversion efficiency, because of the low barrier properties of the gate-insulator system, as shown by Japanese Patent to Hamakawa et al (cf. "Purpose" and "Constitution" in the English summary). Alternatively, from the point of view of well-established physics data on $Si_{1-x}C_x$ the dependence on carbon content of the electron affinity of $Si_{1-x}C_x$ points to a lower electron affinity for SiC (i.e., x=0.5) than for Si (i.e., x=0) so that it can be expected that $Si_{1-x}C_x$ within a neighborhood of x=0.5 can be used to achieve even better results as those obtained with SiC.

6. ***Claims 36-37*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara (5,798,548) in view of Weitzel et al (5,661,312) and Hamakawa et al (JP357126175A).

With regard to claim 36: Fujiwara teaches a transistor comprising: a source region 2, drain region 2, and channel region 3, and a gate 5 formed of polysilicon (cf.

abstract, second sentence and title) separated from the channel region by a thin insulator layer 116 (cf. column 2, line 60 – column 3, line 6). The gate is formed of Fujiwara does not necessarily teach the gate in question to be formed of a silicon carbide compound, although a control gate is taught to be made of silicon carbide. However, as shown by Weitzel et al it has long been known silicon carbide can be used as gate material to achieve better breakdown performance, while Hamakawa et al teach that $Si_{1-x}C_x$ with x>0.5 can be selected as an excellent material for obtaining high electronic conversion efficiency, because of the low barrier properties of the gate-insulator system, as shown by Japanese Patent to Hamakawa et al (cf. "Purpose" and "Constitution" in the English summary). Alternatively, from the point of view of well-established physics data on $Si_{1-x}C_x$ the dependence on carbon content of the electron affinity of $Si_{1-x}C_x$ points to a lower electron affinity for SiC (i.e., x=0.5) than for Si (i.e., x=0) so that it can be expected that $Si_{1-x}C_x$ within a neighborhood of x=0.5 can be used to achieve even better results as those obtained with SiC.

With regard to claim 37: it is clear that ordinary skills can be applied to this art to determine x so as to optimize the desired value of the electron affinity or barrier energy through proper selection of the stoichiometric parameter, with reference to the range for the electrical resistivity cited by Hamakawa et al.

7. ***Claims 36-39*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Weitzel et al (5,661,312).

With regard to claim 36: Weitzel et al teach (cf. Figure on front page) in their claim 10 a transistor (their claim 1: a silicon carbide MOSFET) comprising: a source region at and near 22, drain region at and near 14, and channel region 14 (cf. column 1, line 40 –column 2, line 12) between the source and drain regions, and a gate 18 separated from the channel by an insulator 17 (for example: silicon dioxide; cf. column 1, line 52), the gate formed of a silicon carbide compound (cf. column 4, lines 6-8). Weitzel does not necessarily teach the silicon carbide to be $Si_{1-x}C_x$ with x>0.5 to establish a desired value of the barrier energy between gate and insulator. However, within the context of the invention taught by Weitzel et al it would have been obvious to increase the carbon content to a value x greater than 0.5 because the purpose of the invention by Weitzel is to increase the breakdown voltage: by increasing the carbon content to x > 0.5 the resistivity of $Si_{1-x}C_x$ is increased whereby the electrical breakdown threshold of the gate material, interposed between the gate electrode (not shown; cf. column 1, line 67) and the drain (cf. column 2, line 14-16), would be increased. The limitation "to establish a desired value of a barrier energy" pertains only to the use of the device and not the device itself. Therefore, said limitation is irrelevant for the device invention of Applicant.

With regard to claim 37: that x is to be "selected at a predetermined value" is just common practice because it is understood that device parameters are arrived at after some optimization effort.

With regard to claims 38-39: The said barrier energy varies between –1.3 eV at x=1 and approximately 2.8 eV at x=0.5, as disclosed by Applicant's summary of well-

known physics data through Figures 3A-3C using silicon dioxide as the insulator material (said Figures do not pertain to the invention itself). Weitzel et al teach a gate insulation layer 17 made of silicon dioxide (cf. column 1, line 52). Therefore, the further limitations of claims 38-39 are automatically satisfied by the limitation defined by claim number 36.

8. ***Claims 41-44*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara as applied to claim 40, in view of Miyawaki (5,808,336). The intergate dielectric taught by Fujiwara is not specifically taught to be formed of silicon dioxide. However, it would have been obvious to one of ordinary skills to proscribe that said intergate dielectric film be made of silicon dioxide, because it is understood that silicon dioxide is an excellent insulator and can be integrated with semiconductor and silicon compound structures in semiconductor memory devices, using thermal oxidation of polysilicon for its easy manufacture, as witnessed by Miyawaki (cf. column 9, lines 1-10) who teaches integrate dielectric film 61 to be so manufatured and constituted.

With regard to claim 42: it is understood that the charge retention time depends on the electron affinity of the floating gate, hence the further limitation of claim 42 is obviously met by selecting the stoichiometric parameter x to adjust the barrier energy between gate and insulator. Therefore, claim 42 does not distinguish over claim 40.

With regard to claim 43: predetermined selection of x determines the band energy as well as the electron affinity, and thereby the photon wavelength range of photons most likely to be absorbed. Therefore, claim 43 is implied by claim 40.

With regard to claim 44: it is understood by those skilled in the art that electron emission by the floating gate in response to incident photons necessarily changes the current conductance between source and drain through a change in the gate voltage and consequent change in the carrier abundance in the channel region. Therefore, claim 44 does not distinguish over claim 43.

9. ***Claim 45*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Weitzel et al as applied to claim 36 above, and further in view of Shrivastava et al (5,557,122). Weitzel et al do not necessarily teach the further limitation defined by claim 45. However, Shrivastava et al teach a floating gate that retains its microcrystalline structure so as to have, inter alia, improved stress induced defect problems (cf. abstract). Stress induced defect problems can be considered generally of concern to field effect transistors, whence motivation is easily established. Combination does not offer problems of any device or method of making nature: the floating gate can be manufactured to be microcrystalline by straightforward application of P-doping (cf. abstract). Reasonable expectation of success is thus valid.

10. ***Claims 36-39*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Weitzel et al (5,661,312) in view of Hamakawa et al (JP357126175A).

With regard to claim 36: Weitzel et al teach (cf. Figure on front page) in their claim 10 a transistor (their claim 1: a silicon carbide MOSFET) comprising: a source region at and near 22, drain region at and near 14, and channel region 14 (cf. column 1,

line 40 –column 2, line 12) between the source and drain regions, and a gate 18 separated from the channel by an insulator 17 (for example: silicon dioxide; cf. column 1, line 52), the gate formed of a silicon carbide compound (cf. column 4, lines 6-8). Weitzel does not necessarily teach the silicon carbide to be $Si_{1-x}C_x$ with x>0.5 to establish a desired value of the barrier energy between gate and insulator. However, the use of $Si_{1-x}C_x$ with x>0.5 as a electrode contact layer with predetermined electrical resistivity to obtain a high photoelectric conversion efficiency (cf. "Purpose", lines 1-3) has long been known and practiced in the art, as witnessed by Japanese Patent to Hamakawa et al (cf. "Constitution", lines 1-18). Resistivity and reflectivity are related, as shown by the well-known Kramers-Kronig relations known to those of ordinary skills in the art of the basic physics of optoelectronics. Obviously, a lower electron affinity is the cause of the improvement of said photoelectric conversion efficiency. Therefore, application of the MOSFET device taught by Weitzel et al to the field of memory and light detection devices would make incorporation of the teaching of Hamakawa et al through the use of a gate layer formed of $Si_{1-x}C_x$ obvious. Such a layer would fit nicely into a silicon carbide device, whence the inventions can be efficiently combined. Also, the art taught by Hamakawa et al has had plenty of time to mature, which justifies reasonable expectation of success. The limitation "to establish a desired value of a barrier energy" pertains only to the use of the device and not the device itself. Therefore, said limitation is irrelevant for the device invention of Applicant.

With regard to claim 37: that x is to be "selected at a predetermined value" is just common practice because it is understood that device parameters are arrived at after some optimization effort.

With regard to claims 38-39: The said barrier energy varies between –1.3 eV at x=1 and approximately 2.8 eV at x=0.5, as disclosed by Applicant's summary of well-known physics data through Figures 3A-3C using silicon dioxide as the insulator material. Weitzel et al teach a gate insulation layer 17 made of silicon dioxide (cf. column 1, line 52). Therefore, the further limitations of claims 38-39 are automatically satisfied by the limitation defined by claim 36.

11. ***Claims 56-57*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara (5,798,548) in view of Weitzel et al (5,661,312) and Hamakawa et al (JP357126175A). Fujiwara teaches (front figure) a transistor comprising a source region 2, drain region 3 (column s and lines previously indicated), both formed in a silicon substrate 1 (cf. column 3, line 67); a channel region 3 in said silicon substrate between the source region and the drain region; and a gate 5 separated from the channel region by an insulator 4, the gate 5 comprising polysilicon. Fujiwara does not necessarily teach the gate 5 to comprise silicon carbide $Si_{1-x}C_x$ with x between 0 and 1. However, silicon carbide gates have long been used in the art to achieve better breakdown voltage of field effect transistors, as witnessed by Weitzel (cf. abstract and claim 10), while Hamakawa et al teach $Si_{1-x}C_x$ with x>0.5 as an electrode contact layer with predetermined electrical resistivity to obtain a high photoelectric conversion efficiency

(cf. "Purpose", lines 1-3) has long been known and practiced in the art, as witnessed by Japanese Patent to Hamakawa et al (cf. "Constitution", lines 1-18). Resistivity and reflectivity are related, as shown by the well-known Kramers-Kronig relations known to those of ordinary skills in the art of the basic physics of optoelectronics. Obviously, said photoelectric conversion efficiency is favorably affected by the lowering of the electron affinity.

With regard to claim 57: the substrate taught by Hamakawa et al is a P-substrate with the obvious advantage of allowing electrons to be the carriers, while in the case of Fujiwara the insulator 59 is an oxide and can obviously be made most efficiently as a thermal oxide film of Si, in other words: silicon dioxide.

12. ***Claim 58*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara, Weitzel et al and Hamakawa et al as applied to claim 56 above, and further in view of Shrivastava et al (5,557,122). Neither Fujiwara nor Weitzel et al nor Hamakawa et al necessarily teach the further limitation defined by claim 58. However, Shrivastava et al teach a floating gate that retains its microcrystalline structure so as to have improved stress induced defect problems (cf. abstract).

13. ***Claim 59*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara (5,798,548) in view of Weitzel et al and Hamakawa (JP357126175A).

Fujiwara teaches (cf. front figure and with reference to previously made column and line citations) a source region 2 in a substrate 1, a drain region 2 in a substrate, a

channel region 3 in a substrate between the source and the drain, and a gate 5 separated from the channel region by an insulator 4, the gate 5 comprising polysilicon and not necessarily silicon carbide compound $Si_{1-x}C_x$ with x between 0.5 and 1.0. However, the use of silicon carbide gates in the art of field effect transistors to achieve better breakdown performance is evident from Weitzel et al (cf. abstract and claim 10). Furthermore, $Si_{1-x}C_x$ with x>0.5 as an electrode contact layer with predetermined stoichiometric composition to lower the electron affinity has long been known and practiced in the related art of photoelectronic conversion, as witnessed by Japanese Patent to Hamakawa et al (cf. "Constitution", lines 1-18). Obviously, the photoelectric conversion efficiency is favorably affected by the lowering of the electron affinity.

14. ***Claims 60-61*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara, Weitzel et al and Hamakawa et al as applied to claim 59 above, and further in view of Miyawaki (5,808,336).

With regard to claim 60: As detailed above, claim 59 is unpatentable over Fujiwara in view of Weitzel et al and Hamakawa et al, who, while Fujiwara teaches the substrate to be made of silicon (cf. column 3, line 67). Fujiwara does not necessarily teach the silicon substrate to be a p-type substrate. However, the substrate taught by Hamakawa et al is a p-substrate with the obvious advantage of allowing electrons to be the carriers, while in the case of Fujiwara the insulator 59 is an oxide and can obviously be made most efficiently as a thermal oxide film of Si, in other words: silicon dioxide.

With regard to claim 61: Neither Fujiwara, nor Weitzel et al nor Hamakawa et al necessarily teach the further limitation of claim 61. However, Shrivastava et al teach a floating gate that retains its microcrystalline structure so as to have improved stress induced defect problems (cf. abstract).

15. ***Claims 62 and 65*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara (5,798,548) in view of Halvis et al (5,369,040).

With regard to claim 62: As detailed above, and referring to the column and line citations previously made, Fujiwara teaches a transistor (cf. front figure) comprising a source region 2 formed in a substrate 1, a drain region 2 formed in a substrate, a channel region 3 formed between the source and drain regions, and a gate 5 separated from the channel region by an insulator 4, the gate 5 comprising polysilicon rather than a silicon carbide compound $Si_{1-x}C_x$. However, when as in imaging arrays the objective of the device just calls for a reduction in the longwave cutoff of the gate material for transparency a small amount of carbon introduced in silicon is both necessary for the desired effect and enough, as witnessed by Halvis et al, who teach adding up to 50% carbon, preferably about 10% carbon, to silicon (cf. abstract and column 3, lines 13-15 and Table 1). The inventions by Fujiwara and Halvis et al can be combined as nothing else would have to be modified in the basic transistor design, except for the carbon content. The motivation for lowering the carbon content stems from the cost of introducing the carbon. The process of making the device is actually simplified and

shortened so that reasonable expectation of success in the combination of the invention is assured.

With regard to claim 65: Halvis et al teach a range for x that considerably intersects with the range of the claim, as discussed above under claim 62.

16. ***Claims 63-64*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara and Halvis et al as applied to claim 62 above, and further in view of Miyawaki (5,808,336).

With regard to claim 63: As detailed above, claim 62 is unpatentable over Fujiwara in view of Halvis et al, who, however, do not necessarily teach the silicon substrate to be a p-substrate. Also, neither do Forbes et al or Halvis et al show the insulator to comprise a layer of silicon dioxide. However, the substrate taught by Hamakawa et al is a p-substrate with the obvious advantage of allowing electrons to be the carriers, while in the case of Fujiwara the insulator 59 is an oxide and can obviously be made most efficiently as a thermal oxide film of Si, in other words: silicon dioxide.

With regard to claim 64: Neither Fujiwara nor Hamakawa et al necessarily teach the further limitation of claim 61. However, Shrivastava et al teach a floating gate that retains its microcrystalline structure so as to have improved stress induced defect problems (cf. abstract).

17. ***Claims 66-67*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara and Halvis et al as applied to claim 65 above, and further in view of Miyawaki

(5,808,336). Fujiwara teaches the substrate to be a silicon substrate while, for superior mobility of the charge carriers in the channel a P-type substrate is obviously preferable in the case of silicon, because the electron mobility exceeds the hole mobility. Neither do Forbes et al or Halvis et al show the insulator to comprise a layer of silicon dioxide. However, Miyawaki does teach said insulator to be formed by thermal oxidation of polysilicon, hence to be made of silicon dioxide (cf. column 8, line 57). Furthermore, silicon dioxide is widely used as gate insulation layer for its excellent insulator properties, and hence combinability of the inventions is guaranteed with reasonable expectation of success.

With regard to claim 67: Neither Fujiwara, Halvis et al, nor Miyawaki necessarily teach the further limitation of claim 67. However, Shrivastava et al teach a floating gate that retains its microcrystalline structure so as to have improved stress induced defect problems (cf. abstract).

18. ***Claim 68*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara (5,798,548) in view of Weitzel et al and Hamakawa et al (JP357126175A), or in the alternative, in view of Halvis et al (5,369,040). As amply explained in the discussion of previous claims, and with reference therefore to the columns and lines provided in said previous discussions: Fujiwara teaches a floating gate transistor comprising a source region 2, drain region 2, both formed in a silicon substrate 1, a channel region 3 in said semiconductor substrate between source and drain regions, a floating gate 5 separated from the channel region by an insulator 4; the floating gate comprising polysilicon rather

than a silicon carbide compound $Si_{1-x}C_x$ with x selected between 0 and 1; and a control gate 7 separated from the floating gate 5 by an intergate dielectric 6. However, when as in imaging arrays the objective of the device just calls for a reduction in the longwave cutoff of the gate material for transparency a small amount of carbon introduced in silicon is both necessary for the desired effect and enough, as witnessed by Halvis et al, who teach adding up to 50% carbon, preferably about 10% carbon, to silicon (cf. abstract and column 3, lines 13-15 and Table 1). The inventions by Fujiwara and Halvis et al can be combined as nothing else would have to be modified in the basic transistor design, except for the carbon content. The motivation for lowering the carbon content stems from the cost of introducing the carbon. The process of making the device is actually simplified and shortened so that reasonable expectation of success in the combination of the invention is assured. Furthermore, alternatively it is noted that silicon carbide gates have long been applied to achieve better breakdown characteristics in field effect transistors, as witnessed by Weitzel et al, while it has long been known that $Si_{1-x}C_x$ with $x>0.5$ can be selected as an excellent material for obtaining high electronic conversion efficiency in the related field of optoelectronic devices, because of the low barrier properties of the electrode-insulator system, as shown by Japanese Patent to Hamakawa et al (cf. "Purpose" and "Constitution" in the English summary). Also, from the point of view of well-established physics data on $Si_{1-x}C_x$ the dependence on carbon content of the electron affinity of $Si_{1-x}C_x$ points to a lower electron affinity for SiC (i.e., $x=0.5$) than for Si (i.e., $x=0$) so that it can be expected that $Si_{1-x}C_x$ within a neighborhood of $x=0.5$ can be used to achieve even better results as those obtained with SiC.

19. ***Claim 69*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara and Halvis, or, in the alternative, over Fujiwara, Weitzel et al and Hamakawa et al as applied to claim 68 above, and further in view of Miyawaki (5,808,336). Although Fujiwara nor Halvis et al nor Weitzel et al nor Hamakawa et al necessarily show the insulator separating the floating gate and the channel, nor the integrate insulator, to comprise silicon dioxide, it is generally understood in the art that silicon dioxide is a very good interlayer dielectric and hence it is not surprising that Miyawaki teaches both insulator layers 59 and 62 to be made by thermal oxidation of silicon, hence necessarily to be made of silicon oxide, said thermal oxidation also being an efficient processing method, in view of the presence of silicon.

20. ***Claim 70*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara, Halvis et al, and Miyawaki, or, in the alternative Fujiwara, Weitzel et al, Hamakawa et al and Miyawaki as applied to claim 69 above, and further in view of Shrivastava et al (5,557,122). Neither Fujiwara, Halvis et al nor Weitzel et al nor Hamakawa et al, nor Miyawaki necessarily teach the further limitation of claim 70. However, Shrivastava et al teach a floating gate that retains its microcrystalline structure so as to have improved stress induced defect problems (cf. abstract).

21. ***Claims 71, 80, and 83*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara (5,798,548) in view of Weitzel et al (5,661,312) and

Hamakawa et al (JP357126175A). The limitations of claims 71, 80, and 83 not necessarily met by Fujiwara are restricted those pertaining to the value of x be in the range between 0.5 and 1.0, or in the range between 0.5 and 0.75, or in the range between 0.75 and 1.0, respectively. However, it has long been known silicon carbide gates improve breakdown performance of field effect transistors, while in the related field of optoelectronic devices it has long been known that $Si_{1-x}C_x$ with $x>0.5$ can be selected as an excellent material for obtaining high optoelectronic conversion, because of the low barrier properties of the gate-insulator system, as shown by Japanese Patent to Hamakawa et al (cf. “Purpose” and “Constitution” in the English summary). Alternatively, from the point of view of well-established physics data on $Si_{1-x}C_x$ the dependence on carbon content of the electron affinity of $Si_{1-x}C_x$ points to a lower electron affinity for SiC (i.e., x=0.5) than for Si (i.e., x=0) so that it can be expected that $Si_{1-x}C_x$ within a neighborhood of x=0.5 can be used to achieve even better results as those obtained with SiC and, moreover, with a compound that is simpler to manufacture.

22. ***Claims 72-73, 81-82, and 84-85*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara, Weitzel et al and Hamakawa et al as applied to claims 71 and 80 above, and further in view of Miyawaki et al (5,808, 336).

With regard to claims 72, 81, and 84: it is generally understood in the art that silicon dioxide is a very good interlayer dielectric and hence it is not surprising that Miyawaki teaches both insulator layers 59 and 62 to be made by thermal oxidation of

silicon, hence necessarily to be made of silicon oxide. Fujiwara teaches the use of silicon for the substrate.

23. *With regard to claims 73, 82, and 85:* Neither Fujiwara, nor Weitzel et al, nor Hamakawa et al, nor Miyawaki necessarily teach the further limitation of claim 70. However, Shrivastava et al teach a floating gate that retains its microcrystalline structure so as to have improved stress induced defect problems (cf. abstract).

24. ***Claims 74, 76-77 and 79*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara (5,798,548) in view of Halvis et al (5,369,040).

With regard to claims 74 and 77: As detailed above, Fujiwara teach a transistor comprising a source region 2 formed in a substrate 1, a drain region 2 formed in a substrate, a channel region 3 formed between the source and drain regions, and a gate 5 separated from the channel region by an insulator 4, the gate 5 comprising polysilicon rather than a carbide compound $Si_{1-x}C_x$. However, when as in imaging arrays the objective of the device just calls for a reduction in the longwave cutoff of the gate material for transparency a small amount of carbon is enough, as witnessed by Halvis et al, who teach adding up to 50% carbon, preferably about 10% carbon, to silicon (cf. abstract and column 3, lines 13-15 and Table 1) for the specific purpose of increasing visibility to light of gates in applications to imaging MOSFET arrays. The inventions by Fujiwara and Halvis et al can be combined as nothing else would have to be modified in the basic transistor design, except for the carbon content in the polysilicon gate 5.

25. ***Claims 76 and 79*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara and Halvis et al as applied to claims 74 and 77 above, and further in view of Shrivastava et al (5,557,122). Neither Fujiwara, nor Halvis et al necessarily teach the further limitation of claims 76 and 79. However, Shrivastava et al teach a floating gate that retains its microcrystalline structure so as to have improved stress induced defect problems (cf. abstract).

26. ***Claims 75 and 78*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara and Halvis et al as applied to claims 74 and 77 above, and further in view of Miyawaki (5,808,336). Fujiwara teach the substrate to be a silicon substrate, as mentioned before. Although Fujiwara does not necessarily teach the silicon substrate to be a p-substrate, p-type substrates in silicon-based transistor art should be preferred because of the electron mobility exceeds the hole mobility. Furthermore, although neither Fujiwara nor Halvis et al necessarily teach the insulator to comprise a layer of silicon dioxide, Miyawaki does teach said layer to be formed by thermal oxidation of polysilicon, hence to be made of silicon dioxide (cf. column 8, line 57). Furthermore, silicon dioxide is widely used as gate insulation layer for its excellent insulator properties, while silicon dioxide can be made from silicon by thermal oxidation; hence combinability of the inventions is guaranteed with reasonable expectation of success.

27. ***Claim 98*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara, Weitzel et al, and Hamakawa et al as applied to claim 36 above, and further in

view of Miyawaki (5,808,336). As detailed above, claim 36 is unpatentable over Fujiwara in view of Weitzel et al and Hamakawa et al. Fujiwara teaches the floating gate 5 to be separated from the control gate 7 by an intergate dielectric 6. Neither Fujiwara nor Hamakawa et al necessarily teach an intergate dielectric made of silicon dioxide. However, it is generally understood in the art that silicon dioxide is a very good interlayer dielectric and hence it is not surprising that Miyawaki teaches both insulator layers 59 and 62 to be made by thermal oxidation of silicon, hence necessarily to be made of silicon oxide, especially in view of the efficiency with which silicon dioxide can be made in silicon through thermal oxidation.

28. ***Claim 99*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara, Weitzel et al and Hamakawa et al as applied to claim 37 above, and further in view of Miyawaki (5,808,336) and Shrivastava et al (5,557,122). Neither Fujiwara nor Hamakawa et al necessarily teach an insulator made of silicon dioxide. However, it is generally understood in the art that silicon dioxide is a very good insulators and hence it is not surprising that Miyawaki teaches both insulator layers 59 and 62 to be made by thermal oxidation of silicon, hence necessarily to be made of silicon oxide, especially in view of the efficiency with which silicon dioxide can be made in silicon through thermal oxidation. Furthermore, although neither Fujiwara nor Weitzel et al nor Hamakawa et al necessarily teach the material for the gate to be selected out of the set enumerated in claim 99, Shrivastava et al teach a floating gate that retains its microcrystalline structure so as to have improved stress induced defect problems (cf. abstract).

29. ***Claim 100*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara, Weitzel et al and Hamakawa et al as applied to claim 40 above, and further in view of Miyawaki (5,808,336) and Shrivastava et al (5,557,122). Neither Fujiwara nor Weitzel et al nor Hamakawa et al necessarily teach the further limitation defined by claim 100. However, it is generally understood in the art that silicon dioxide is a very good insulators and hence it is not surprising that Miyawaki teaches both insulator layers 59 and 62 to be made by thermal oxidation of silicon, hence necessarily to be made of silicon oxide, especially in view of the efficiency with which silicon dioxide can be made in silicon through thermal oxidation. Furthermore, although neither Fujiwara nor Hamakawa et al necessarily teach the material for the gate to be selected out of the set enumerated in claim 99, Shrivastava et al teach a floating gate that retains its microcrystalline structure so as to have improved stress induced defect problems (cf. abstract).

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Malhi (5,393,999); Fujii et al (JP402203564A); Ohba (5,734,181).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
May 15, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800